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Request for Continued Examination (RCE) Transmittal

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Application Number	10/643,967
Filing Date	August 20, 2003
First Named Inventor	Hiroyuki NANSEI et al.
Art Unit	2822
Examiner Name	Thomas, TONIAE M.
Attorney Docket Number	030993

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Rely Brief previously filed on _____

      ii. ☐ Other _____

   b. ☑ Enclosed

      i. ☑ Amendment/Reply

      ii. ☐ Affidavit(s)/ Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☑ Other Petition for Extension of Time

2. Miscellaneous

   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☑ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-2866

      i. ☐ RCE fee required under 37 CFR 1.17(e)

      ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☑ Other any check insufficiency or additional fee

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   02 FC:1801 790.00 OP

   b. ☑ Check in the amount of $ 910.00(790+120) enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Sadao Kinashi	*Registration No. (Attorney/Agent)*	48,075
Signature	Sadao Kinashi	*Date*	April 4, 2005

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Hiroyuki NANSEI et al.** Group Art Unit: **2822**

Serial No.: **10/643,967** Examiner: **Toniae M. Thomas**

Filed: **August 20, 2003** Confirmation No.: **4992**

For: **SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE**

Attorney Docket Number: **030993**
Customer Number: **38834**

SUBMISSION UNDER 37 C.F.R. §1.114

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Date: April 4, 2005

Sir:

This Submission is being filed concurrently with a Request for Continued Examination pursuant to 37 C.F.R. §1.114.

Amendments to the Claims are reflected in the listing of claims that begins on page 2 of this paper.

Remarks/Arguments begin on page 12 of this paper.

AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions of claims in the application.

Listing of Claims:

1. (Currently amended): A method for manufacturing a semiconductor device, comprising:

a step of forming a lower silicon oxide film;

a step of forming a silicon film on the lower silicon oxide film; ~~and~~

a step of forming a silicon nitride film on the lower silicon oxide film to completely nitride the silicon film with a surface wave plasma generated by a plasma nitriding method, wherein a multilayered insulating film including at least the lower silicon oxide film and the silicon nitride film is formed; and

a step of forming an upper silicon oxide film to oxidize a surface of the silicon nitride film by a plasma oxidizing method,

wherein the multilayered insulating film composed of the lower silicon oxide film, the silicon nitride film, and the upper silicon oxide film is formed.

2. (Cancelled).

3. (Currently amended): The method for manufacturing the semiconductor device according to ~~claim 1~~ claim 39, wherein

the silicon film is formed under a temperature condition of 700°C or below.

4. (Currently amended): The method for manufacturing the semiconductor device according to ~~claim 1~~ claim 39, wherein the silicon nitride film is a charge-storage film of a memory cell.

5. (Currently amended): The method for manufacturing the semiconductor device according to ~~claim 2~~ claim 1, wherein the multilayered insulating film is formed as a dielectric film provided between a floating gate and a control gate in a memory cell.

6. (Currently amended): The method for manufacturing the semiconductor device according to ~~claim 2~~ claim 1, wherein a gate insulation film composed of a silicon oxide film only is formed in a peripheral circuit region by the plasma oxidizing method simultaneously with the upper silicon oxide film.

7. (Original): The method for manufacturing the semiconductor device according to claim 1, wherein a film thickness of the silicon film is 5 nm or above.

8. (Currently amended): The method for manufacturing the semiconductor device according to ~~claim 1~~ claim 39, wherein the silicon nitride film is formed by conducting nitriding processing in which plasma is excited by microwave in an atmosphere of a source gas containing nitrogen to generate a nitrogen radical.

9. (Original): The method for manufacturing the semiconductor device according to claim 8, wherein the source gas does not contain hydrogen.

10. (Currently amended): The method for manufacturing the semiconductor device according to ~~claim 2~~ claim 1, wherein the upper silicon oxide film is formed by conducting oxidizing processing in which plasma is excited by microwave in an atmosphere of a source gas containing oxygen to generate an oxygen radical.

11. (Original): The method for manufacturing the semiconductor device according to claim 10, wherein the source gas does not contain hydrogen.

12. (Withdrawn): A method for manufacturing a semiconductor device, comprising:

a step of forming a silicon nitride film to nitride a surface of a silicon region by a plasma nitriding method; and

a step of oxidizing a surface of a silicon nitride film and an interface of the surface of the silicon region facing with the silicon nitride film simultaneously by a plasma oxidizing method, and of simultaneously forming an upper silicon oxide film on the surface thereof and a lower silicon oxide film on the interface thereof, wherein

a multilayered insulating film composed of the lower silicon oxide film, the silicon nitride film and the upper silicon oxide film is formed.

13. (Withdrawn): The method for manufacturing the semiconductor device according to claim 12, wherein the silicon region is an island-shaped floating gate formed in every memory cell, and the multilayered insulating film is a dielectric film provided between the floating gate and a control gate in the memory cell.

14. (Withdrawn): The method for manufacturing the semiconductor device according to claim 12, wherein the silicon region is a semiconductor substrate and the multilayered insulating film is a charge-storage film of the memory cell, and further comprising:

a step of forming a gate electrode on the multilayered insulating film after the multilayered insulating film is formed.

15. (Withdrawn): The method for manufacturing the semiconductor device according to claim 12, wherein a gate insulation film is formed in a peripheral circuit region by the plasma oxidizing method simultaneously with the silicon oxide film.

16. (Withdrawn): The method for manufacturing the semiconductor device according to claim 12, wherein a film thickness of the silicon nitride film formed by the plasma nitriding method is 15 nm or below.

17. (Withdrawn): The method for manufacturing the semiconductor device according to claim 12, wherein the silicon nitride film is formed by conducting nitriding processing in which

plasma is excited by microwave in an atmosphere of a source gas containing nitrogen to generate a nitrogen radical.

18. (Withdrawn): The method for manufacturing the semiconductor device according to claim 17, wherein the source gas does not contain hydrogen.

19. (Withdrawn): The method for manufacturing the semiconductor device according to claim 12, wherein the silicon oxide film is formed by conducting oxidizing processing in which plasma is excited by microwave in an atmosphere of a source gas containing oxygen to generate an oxygen radical.

20. (Withdrawn): The method for manufacturing the semiconductor device according to claim 19, wherein the source gas does not contain hydrogen.

21. (Withdrawn): A method for manufacturing a semiconductor device, comprising:

a step of forming a lower silicon oxide film;

a step of forming a silicon nitride film on the lower silicon oxide film by a CVD method; and

a step of oxidizing a surface of the silicon nitride film by a plasma oxidizing method, wherein

a multilayered insulating film composed of the lower silicon oxide film, the silicon nitride film and an upper silicon oxide film is formed.

22. (Withdrawn): The method for manufacturing the semiconductor device according to claim 21, wherein the silicon nitride film is a charge-storage film of a memory cell.

23. (Withdrawn): The method for manufacturing the semiconductor device according to claim 21, wherein the multilayered insulating film is formed as a dielectric film provided between a floating gate and a control gate in the memory cell.

24. (Withdrawn): The method for manufacturing the semiconductor device according to claim 21, wherein a gate insulation film is formed in a peripheral circuit region by the plasma oxidizing method simultaneously with the upper silicon oxide film.

25. (Withdrawn): The method for manufacturing the semiconductor device according to claim 21, wherein a film thickness of the silicon nitride film formed by the CVD method is 5 nm or above.

26. (Withdrawn): The method for manufacturing the semiconductor device according to claim 21, wherein the silicon nitride film is formed by conducting nitriding processing in which plasma is excited by microwave in an atmosphere of a source gas containing nitrogen to generate a nitrogen radical.

27. (Withdrawn): The method for manufacturing the semiconductor device according to claim 26, wherein the source gas does not contain hydrogen.

28. (Withdrawn): The method for manufacturing the semiconductor device according to claim 21, wherein the upper silicon oxide film is formed by conducting oxidizing processing in which plasma is excited by microwave in an atmosphere of a source gas containing oxygen to generate an oxygen radical.

29. (Withdrawn): The method for manufacturing the semiconductor device according to claim 28, wherein the source gas does not contain hydrogen.

30. (Withdrawn): A semiconductor memory device, comprising:

a memory cell; including

a semiconductor substrate,

an insulation film including a silicon nitride film having a charge-capture function, formed on the semiconductor substrate,

a gate electrode formed on the semiconductor substrate via the insulation film, and

a pair of impurity diffused layers formed on the semiconductor substrate, wherein

the silicon nitride film is a uniform and dense nitrided film formed by only plasma nitriding through microwave excitation or a series of processing including the plasma nitriding.

31. (Withdrawn): The semiconductor memory device according to claim 30, wherein the insulation film is a multilayered insulating film composed of a silicon nitride film on a lower silicon oxide film.

32. (Withdrawn): The semiconductor memory device according to claim 30, wherein the insulation film is a multilayered insulating film composed of the lower silicon oxide film, the silicon nitride film, and an upper silicon oxide film.

33. (Withdrawn): The semiconductor memory device according to claim 31, wherein either or both of the lower silicon oxide film and/or the upper silicon oxide film is/are (a) uniform and dense oxide film(s) formed by plasma oxidization through microwave excitation.

34. (Withdrawn): The semiconductor memory device according to claim 33, wherein a gate insulation film of a transistor as a component of a peripheral circuit is a uniform and dense oxide film formed by plasma oxidization through microwave excitation, and simultaneously formed with the upper silicon oxide film.

35. (Withdrawn): A semiconductor memory device, comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

an island-shaped floating gate having a charge-capture function, the charge-capture function being formed on said semiconductor substrate via said insulation film;

a dielectric film formed on said floating gate;

a control gate formed on said floating gate via said dielectric film; and

a pair of impurity diffused layers formed on said semiconductor substrate, wherein

said dielectric film includes a uniform and dense silicon nitride film formed by only plasma nitriding through microwave excitation or a series of processing including the plasma nitriding.

36. (Withdrawn): The semiconductor memory device according to claim 35, wherein said dielectric film is a multilayered insulating film composed of the silicon nitride film formed on a lower silicon oxide film.

37. (Withdrawn): The semiconductor memory device according to claim 35, wherein said dielectric film is a multilayered insulating film composed of the lower silicon oxide film, the silicon nitride film, and an upper silicon oxide film.

38. (Withdrawn): The semiconductor memory device according to claim 36, wherein either or both of the lower silicon oxide film and/or the upper silicon oxide film is/are (a) uniform and dense oxide film(s) formed by plasma oxidization through microwave excitation.

39. (Previously presented): A method for manufacturing a semiconductor device, comprising:

a step of forming a lower silicon oxide film;

a step of forming a silicon film on the lower silicon oxide film; and

a step of forming a silicon nitride film on the lower silicon oxide film to completely nitride the silicon film by a plasma nitriding method, wherein a multilayered insulating film including at least the lower silicon oxide film and the silicon nitride film is formed,

wherein a film thickness of the silicon film is 5 nm or above.

40. (Previously presented): A method for manufacturing a semiconductor device, comprising:

a step of forming a lower silicon oxide film;

a step of forming a silicon film on the lower silicon oxide film;

a step of forming a silicon nitride film on the lower silicon oxide film to completely nitride the silicon film by a plasma nitriding method, wherein a multilayered insulating film including at least the lower silicon oxide film and the silicon nitride film is formed; and

a step of forming an upper silicon oxide film to oxidize a surface of the silicon nitride film by a plasma oxidizing method,

wherein the multilayered insulating film composed of the lower silicon oxide film, the silicon nitride film, and the upper silicon oxide film is formed, and

wherein a gate insulation film composed of a silicon oxide film only is formed in a peripheral circuit region by the plasma oxidizing method simultaneously with the upper silicon oxide film.

REMARKS

Allowed Claims

Applicants gratefully acknowledge that claims 39-40 have been allowed.

Allowable Claims

Applicants gratefully acknowledge that claims 2, 5-7 and 10-11 were merely objected to as depending from a rejected base claim, but are otherwise allowable.

Claims 2 has been incorporated into independent claim 1, which has become in condition for allowance. Claims 5-7 and 10-11 have been amended to depend from amended claim 1, now in condition for allowance.

Rejections under 35 USC §103(a)

Claims 1, 3, 8 and 9 were rejected under 35 USC §103(a) as being obvious over Weimer (US 2003/0040171 A1) in view of Chua et al. (US 2004/0038486 A1) .

Claim 1 has been amended to incorporate the recitations of allowed claim 2.

Claims 3, 8 and 9 have been amended to depend from allowed claim 39.

Thus, all pending claims are in condition for allowance. Reconsideration of the rejections, withdrawal of the rejections and objections and an early issue of a Notice of Allowance are earnestly solicited.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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